In the Claims

1. (Currently Amended) A method of forming an interconnection line in a semiconductor device comprising:

forming a first etching stopper on a lower conductive layer which is formed on a semiconductor substrate;

forming a first interlayer insulating layer on the first etching stopper;

forming a second etching stopper on the first interlayer insulating layer;

forming a second interlayer insulating layer over the [first] second etching stopper;

etching the second interlayer insulating layer, the second etching stopper and the first interlayer insulating layer sequentially using the first etching stopper as an etching stopping point to form a via hole aligned with the lower conductive layer;

forming a protective layer to protect a portion of the first etching stopper exposed at the bottom of the via hole, the protective layer filling the via hole and extending across the via hole;

etching the protective layer such that the protective layer remains only in the bottom of the via hole;

after etching the protective layer such that the protective layer remains only in the bottom of the via hole, forming an etching mask on the second interlayer insulating layer;

etching a portion of the second interlayer insulating layer adjacent to the via hole using the second etching stopper as an etching stopping point and the etching mask to form a trench connected to the via hole;

removing the protective layer;

removing the portion of the first etching stopper positioned at the bottom of the via hole; and

forming an upper conductive layer that fills the via hole and the trench and is

electrically connected to the lower conductive layer.

2. (Original) The method of claim 1, wherein the lower conductive layer includes a copper layer.

3. (Currently Amended) The method of claim 1, wherein the first etching stopper is formed of at least one of silicon nitride and silicon carbide.

4. (Original) The method of claim 1, wherein the first interlayer insulating layer is formed of a material having a low dielectric constant.

5. (Original) The method of claim 4, wherein the material having a low dielectric constant is carbon-doped silicon oxide (SiOC).

6. (Currently Amended) The method of claim [19] 1, wherein the second etching stopper is formed of at least one of silicon nitride and silicon carbide.

7. (Original) The method of claim 1, wherein the second interlayer insulating layer is formed of a material having a low dielectric constant.

8. (Original) The method of claim 7, wherein the material having a low dielectric constant is carbon-doped silicon oxide (SiOC).

9. (Original) The method of claim 1, wherein the protective layer includes nonorgarnic spin-on dielectric (SOD).

10. (Original) The method of claim 9, wherein the nonorganic SOD is Hydrogen silsesQuioxane (HSQ).

11. (Original) The method of claim 1, wherein the step of forming the protective layer comprises:

forming the protective layer on the second interlayer insulating layer to fill the via hole; and

etching back the protective layer so that the upper surface of the protective layer is lower than the upper surface of the second interlayer insulating layer.

12. (Original) The method of claim 11, wherein the etch back is performed by a wet etching method using a resist developer.

13. (Original) The method of claim 12, wherein the resist developer includes a tetramethyl ammonium hydroxide aqueous solution.

14. (Original) The method of claim 11, wherein the etch back is performed by a wet etching method using a HF solution diluted with water.

15. (Original) The method of claim 1, wherein the protective layer is removed by a wet etching method using a resist developer.

16. (Original) The method of claim 15, wherein the resist developer includes tetramethyl ammonium hydroxide aqueous solution.

17. (Original) The method of claim 1, wherein the protective layer is removed by a wet etching method using a HF solution diluted with water.

18. (Original) The method of claim 1, wherein the upper conductive layer includes a copper layer.

19. (Canceled) The method of claim 1, further comprising forming a second etching stopper on the first interlayer insulating layer.

20. (Canceled) The method of claim 19, wherein the etching step further comprises etching the second etching stopper with the second interlayer insulating layer and the first interlayer insulating layer using the first etching stopper as an etching stopping point to form the via hole aligned with the lower conductive layer.

21. (Canceled) The method of claim 19, further comprising etching a portion of the second interlayer insulating layer adjacent to the via hole using the second etching stopper as an etching stopping point to form a trench connected to the via hole.